

**REMARKS**

Claim 1-25 are now pending. Applicant has amended claims 1-4 and added claims 5-25.

The Examiner has objected to the disclosure and requested clarification of certain abbreviations. Applicant has amended the specification to address the Examiner's concerns.

The Examiner has objected to the claims because of an informality in the numbering. Applicant has amended the claims to address the Examiner's concerns.

The Examiner has rejected claims 1-4 under 35 U.S.C. § 102(b) as being anticipated by Wooten '299. Applicant respectfully traverses this rejection.

All the pending claims are directed to executing code when a process enters a system management mode ("SMM"). Claims 1-4 recite "executing code during a system management mode interrupt," and claims 5-25 recite "instructions for a system management mode interrupt routine."

The Examiner believes that Wooten's virtual system mode ("VSM") is the same as a system management mode ("SMM"). Applicant respectfully disagrees. Wooten makes the distinction between VSM and SMM very clear. Wooten describes SMM generally along with its disadvantages at 1:55-3:2. One disadvantage is the overhead of saving and restoring the state of the processor when an SMM interrupt occurs and when returning from an SMM interrupt. Another disadvantage is that access to user memory is limited and/or cumbersome when in SMM.

Wooten's solution is to introduce a new processor mode, referred to as the virtual system mode ("VSM"). Wooten makes it clear that SMM is not VSM. For example, as the Examiner notes Wooten describes that bit 31 of the EFLAGS register is set to 1 to indicate that the processor is in VSM. Applicant has included with this response page 3-14 of the Pentium Processor User's Manual, Volume 3:

Architecture and Programming Manual ("Intel"). (Applicant previously cited portions of this Intel that describe SMM in an IDS.) Figure 3-9 of page 3-14 describes the meaning of the bits of the EFLAGS register in which bit 31 is indicated as reserved. Wooten is suggesting that this reserved bit now be used to indicate that the processor is in VSM. Clearly, if SMM was the same as VSM, then no new bit would need to be defined.

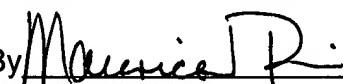
Wooten defines a new mode of the processor to overcome limitations of "the SMM addressing mechanism." (Wooten, 10:25-33.) In particular, when in SMM and emulation is desired, "the user mode addresses must be translated into addresses compatible with the SMM addressing mechanism." (Id.) Wooten explains that "when in virtual system mode, the addressing mechanism of the previous mode of operation can be used for VSM operation, therefore making emulation much simpler." (Wooten, 10:43-46.) Figure 3C of Wooten illustrates that both real and protected mode addressing is available when in VSM. In VSM addresses can be mapped using the segmentation unit and a paging unit. In contrast, Intel describes that SMM uses no "address mapping." (Intel, 20-1.) Wooten clearly indicates the VSM is different from SMM.

Although Wooten's technique and applicant's invention seek to overcome limitations associated with SMM. Wooten technique changes the architecture of the processor to include a new mode—VSM—that avoids the limitations of SMM, whereas applicant's invention works within the existing hardware architecture of the processor with the existing mode—SMM—to overcome limitations by switching mode during execution of an SMM interrupt routine.

Based on the above amendment and remarks, applicant respectfully requests reconsideration of this application and its early allowance. If the Examiner has any questions or believes a telephone conference would expedite prosecution of this application, the Examiner is encouraged to call the undersigned at (206) 359-8548.

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Respectfully submitted,

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